addressing scheme is selected," as claimed in the Application. In the Office Action, Fig. 1, Ref. 38; Col. 5, lines 43-50; Col. 6, lines 14-32; and Col. 7 lines 43-54 of Manning were cited to support the disclosure of such a switching scheme. The Applicants respectfully submit that such is not the case.

First, it should be noted that the Office has admitted that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in another Office Action mailed to the Applicant on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter. If Manning does not disclose these elements, how (specifically) does Manning support *switching* or *selecting* between burst and *pipelined* modes of operation, as claimed in claims 17, 59-61, 64, and 70-71?

Second, the Applicants respectfully draw attention to numerous statements in the instant Office Action which assert that Manning discloses a "control circuit for selecting between an unpatterned pipeline and a patterned burst data pattern," or similar statements (see Paper Nol 25, regarding claims 59-66, and 70-71). The Applicant's representative was unable to find any portion of Manning to support the idea that Manning includes such circuitry, and requests that such support for this proposition be designated with more specificity.

Third, no *prima facie* case of anticipation has been established. The only references offered to support the assertion that Manning "discloses the invention as claimed" with respect to claim 1 are: Fig.1, Ref. 38; col. 5, lines 43-50; col. 6, lines 14-32; and col 7, lines 43-54). Fig. 1, Ref. 38 is a block labeled generic DRAM control logic, with no indication whatsoever regarding exactly which modes may be operative, or how they may be selected. Col. 5, lines 43-50 discuss the possibility of using a pipelined architecture as an *alternative* to burst operation, but not as enabling switching between pipeline or burst operations, on-the-fly, within the *same* memory, as disclosed and claimed by the Applicant. Col. 6, lines 14-32 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Finally, col. 7, lines 43-54 speak to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Manning gives no support whatever to the idea that a pipelined mode of operation is the same as a fast page mode.

Fourth, it is asserted in the Office Action that "... in order to work in the pipeline architecture one has to select pipelined mode." This is not necessarily true, since a memory including a pipeline architecture may operate according to that architecture (which is not the same thing as the pipelined mode) without any switching or selection whatsoever, especially if that is the fixed mode of operation for that memory. Thus, Manning never discusses the ability to *select* between burst and pipelined modes of operation, or patternless and patterned addressing schemes, as claimed by the Applicants in independent claim 11, as well as in independent claims 59-62, 65, 68 and 70, and all of the claims which depend from them.

Finally, the instant Application describes how to switch between data pathways, depending on whether a patternless or patterned addressing scheme is selected. The patternless addressing scheme may include a pipelined extended data out pattern, as in claim 17. It is unreasonable to interpret the possible existence of a pipelined architecture in Manning's device as equivalent to operating in the pipelined mode taught and claimed by the Applicants. It is also inconsistent to admit, on the one hand, that "Manning does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation" in a previous Office Action, and then on the other, to state that Manning teaches control logic and/or switching circuitry to switch between pipelined and burst modes of operation in the instant Office Action. The MPEP requires that "[d]uring patent examination, the pending claims must be 'given the broadest reasonable interpretation consistent with the specification.'" See M.P.E.P. § 2111. The Applicants respectfully submit that the interpretation of the pending claims by the Office is neither reasonable nor consistent with the text of the instant specification.

Thus, what Manning discloses is not identical to the subject matter of the Applicants' invention, and therefore, the rejection under 35 USC § 102 is improper, and should be withdrawn. Reconsideration and allowance of claims 11-21 and 59-71 is therefore respectfully requested.

CONCLUSION

The Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly solicited. The Examiner is invited to telephone The Applicant's attorney, Mark Muller at (210) 308-5677, or the undersigned, to facilitate prosecution of this application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 24 day of October, 2002.

Tina Kohrt
Name

Signature